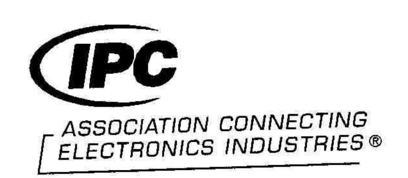


IPC-9701A

Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments

Developed by the SMT Attachment Reliability Test Methods Task Group (6-10d) of the Product and Reliability Committee (6-10) of IPC

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Users of this publication are encouraged to participate in the development of future revisions.

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Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments

1 SCOPE

This specification establishes specific test methods to evaluate the performance and reliability of surface mount solder attachments of electronic assemblies. It further establishes different levels of performance and reliability of the solder attachments of surface mount devices to rigid, flexible and rigid-flex circuit structures. In addition, it provides an approximate means of relating the results from these performance tests to the reliability of solder attachments for the use environments and conditions of electronic assemblies.

1.1 Purpose The purpose of this document is:

- To provide confidence that the design and the manufacturing/assembly processes create a product that is capable of meeting its intended goals.
- To permit the analytical prediction of reliability based on a generic database and technical understanding.
- To provide standardized test methods and reporting procedures.

1.2 Performance Classification This specification recognizes that surface mount assemblies (SMAs) will be subject to variations in performance requirements based on end use. While Performance Classes are defined in IPC-6011, *Generic Performance Specification for Printed Boards,* these performance classifications are not specific as to the required reliability. At this point in time, the reliability requirements need to be established by agreement between customer and supplier.

1.3 Definition of Terms The definition of all terms used herein **shall** be as specified in IPC-T-50, except as otherwise specified in Section 3.

1.4 Interpretation "**Shall**," the imperative form of the verb, is used throughout this specification whenever a requirement is intended to express a provision that is mandatory. Deviation from a "**shall**" requirement may be considered if sufficient data is supplied to justify the exception.

The words "should" and "may" are used whenever it is necessary to express non-mandatory provisions. "Will" is used to express a declaration of purpose."

To assist the reader, the word "**shall**" is presented in bold characters.

1.5 Revision Level Changes Changes made to this revision of the IPC-9701 include Appendix B which establishes guidelines for thermal cycle requirements for Pb-free solder joints. Appendix B provides additional recommendations to existing IPC-9701 section requirements when utilizing a Pb-free soldering process.

2 APPLICABLE DOCUMENTS

The following documents are applicable and constitute a part of this specification to the extent specified herein. Subsequent issues of, or amendments to, these documents will become a part of this specification. Documents are grouped under categories as IPC, Joint Industry Standard, ITRI, EIA and others depending on the source.

2.1 IPC[1]

IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits

IPC-D-279 Design Guidelines for Reliable Surface Mount Technology Printed Board Assemblies

IPC-TM-650 Test Methods Manual[2]

2.1.1	Microsectioning
2.4.1	Adhesion, Plating
2.4.8	Peel Strength, Metal Foil
2.4.21.1	Bond Strength, Surface Mount Land (Perpendicular Pull Method)
2.4.22	Bow and Twist
2.4.36	Rework Simulation, Plated-Through Holes
2.4.41.2	Coefficient of Thermal Expansion, Strain Gage Method
2.5.7	Dielectric Withstanding Voltage, Printed Wiring Material
2.6.5	Physical (Mechanical) Shock, Multilayer Printed Wiring
2.6.7.2	Thermal Shock-Rigid Printed Boards
2.6.8	Thermal Stress, Plated-Through Holes
2.6.9	Vibration, Rigid Printed Wiring

IPC-SM-785 Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments

IPC-S-816 SMT Process Guideline and Checklist

1. www.ipc.org
2. Current and revised IPC Test Methods are available on the IPC website (www.ipc.org/html/testmethods.htm).

IPC-7711/21 Repair and Rework Guide

IPC-9252 Guidelines and Requirements for Electrical Testing of Unpopulated Printed Boards

IPC-9501 PWB Assembly Process Simulation for Evaluation of Electronic Components

IPC-9502 PWB Assembly Soldering Process Guidelines for Electronic Components

IPC-9504 Assembly Process Simulation for Evaluation of Non-IC Components (Preconditioning Non-IC Components)

2.2 Joint Industry Standards[1]

J-STD-001 General Requirements for Soldering Electronic Interconnections

J-STD-002 Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires

J-STD-003 Solderability Tests for Printed Boards

J-STD-020 Moisture-Induced Stress Sensitivity for Classification of Plastic Integrated Circuit Surface Mount Devices

2.3 International Tin Research Institute[3]

ITRI Pub #580 Metallography of Tin and Tin Alloys

ITRI Pub #708 Metallurgy of Solder Joints in Electronics

2.4 Other Publications

2.4.1 Electronic Industries Association[4]

JESD22-A104-B "Temperature Cycling," July 2000

JESD22-B117 "BGA Ball Shear," July 2000

2.4.2 OEM Working Group[5]

SJR-01 Rev. 2 "Solder Joint Reliability Test Standard," February 2001

3 TERMS, DEFINITIONS AND CONCEPTS

3.1 General To assure the reliability of the solder attachment of surface mounted electronic components to a circuit board substrate requires the utilization of Design for Reliability (DfR)-procedures (see IPC-D-279), **and in some cases verification by** testing to qualify a product for specific product categories and environments. The more complex the components or the assembly, the more testing may be necessary to verify reliability.

During use, surface mount solder attachments can be subjected to a variety of loading conditions which can lead to premature failure. The underlying assumption is that the solder joints have been properly wetted, forming a good metallurgical bond between the solder and the base metal of the component build and Printed Wiring (Circuit) Board (PWB/PCB). This assures that early failures are not infant-mortalities due to defective solder joints.

The following load conditions could exist either singly, sequentially or simultaneously and combine to be large enough to cause SMT solder joint failure:

a) Differential thermal expansion.
b) Vibration (transport).
c) Thermal shock (rapid temperature change causing transient differential warpages) during cooling from soldering operation or from severe use environments.
d) Mechanical shock (high acceleration) from severe use conditions or accidental misuse.

The reliability of a surface mount device mounted on a circuit board is a function of solder attachment integrity and device/board interactions. Thermomechanical loading of the package, imposed by the PWB through the soldered interconnects, may cause failures in other areas of the package. The component-level testing in a socket does not provide representative part-on-board loading. The increased usage of non-wirebond die interconnects for numerous CSP constructions and high lead count BGA packages may increase the likelihood of "unexpected" internal component failures during board-level testing.

To ascertain that the solder attachment of surface mount circuit assemblies meet reliability expectations in the intended use environments, it is often necessary to confirm the reliability for some specific applications even after appropriate design for reliability (DfR) measures have been taken. Because of the time-dependent creep and stress relaxation characteristics of solder, the fatigue damage and fatigue life in accelerated testing are not generally equivalent to those in operational use, but product reliability estimates can be obtained from accelerated test results through the use of appropriate acceleration factors.

3.2 Reliability Concepts In the context of this document it is important to have a working definition of reliability, as well as good understanding of the physics-of-failure and statistical failure distribution.

3. www.itri.co.uk
4. www.eia.org
5. OEM Working Group. An informal working group of original equipment manufacturers (OEMs), Agilent Technologies, Cisco Systems, Dell, Hewlett-Packard, IBM, Lucent Technologies, Nortel Networks and Sun Microsystems.

3.2.1 Reliability Definition The ability of a product (surface mount solder attachments) to function under given conditions and for a specified period of time without exceeding acceptable failure levels.

3.3 Physics-of-Failure Concepts

3.3.1 Creep The time-dependent visco-plastic deformation as a function of applied stress and temperature.

3.3.2 Stress Relaxation The time-dependent visco-plastic deformation decreasing the stress by converting elastic strains into plastic strains for solder.

3.3.3 Solder Creep-Fatigue Model Analytical models based on empirical data that estimate the life of solder joints subjected to cyclic creep-fatigue. The estimates of reliability test results, product reliability, and the acceleration factors in this document can be determined with the Engelmaier-Wild model (see IPC-D-279, Appendix A-3.1) or some other suitable proven model.

In the Engelmaier-Wild solder fatigue model a variable fatigue ductility exponent defines the characteristic slope of the curve which correlates fatigue life with the cyclic visco-plastic strain energy experienced by the solder. This exponent is empirically determined and is a function of time and temperature in contrast to the constant exponent used for the Coffin-Manson equation, which was developed for non-creeping metals.

3.3.4 Differential Thermal Expansion The difference in thermal expansion and contractions between materials which occurs as a result of temperature changes encountered during operational use or testing for reliability. Thermal expansions or contractions are defined by the materials' coefficient of thermal expansion (CTE). Two (2) forms of differential thermal expansion are recognized:

1) The "global" thermal expansion mismatch, which is the thermal expansion mismatch between components and substrates.
2) The "local" thermal expansion mismatch, which is the thermal expansion mismatch between the solder itself and the materials to which it is bonded.

3.4 Test Parameters Note: Any definition denoted with an asterisk (*) is a reprint of the term defined in JESD22-A104-B.

3.4.1 *Working Zone The volume in the chamber in which the temperature of the load is controlled within the specified conditions.

3.4.2 Cyclic Temperature Range/Swing The difference between maximum and minimum temperatures incurred during operational use or temperature cycling tests. See Figure 3-1, Table 3-1 and Table 4-1.

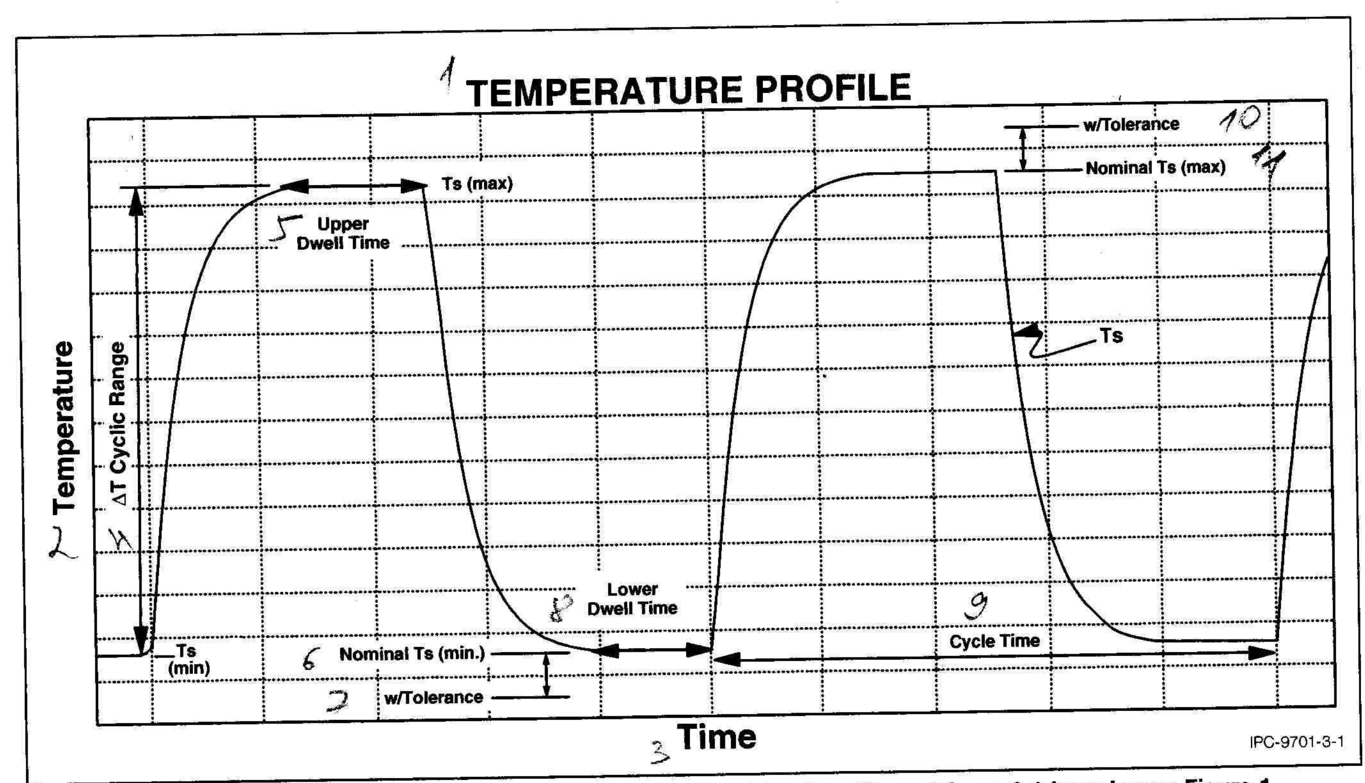


Figure 3-1 Representative Temperature Profile for Thermal Cycle Test Conditions (Figure 3-1 based upon Figure 1, Annex A of JESD22-A104-B)

Table 3-1 Product Categories and Worst-Case Use Environments for Surface Mounted Electronics (For Reference Only)

Product Category (Typical Application)	Temperature, °C / °F[1]		Worst-Case Use Environment						
	Storage	Operation	Tmin[2] °C / °F	Tmax[2] °C / °F	ΔT[3] °C / °F	t_D[4] hrs	Cycles/year	Typical years of Service	Approx. Accept. Failure Risk, %
Consumer	-40/85	0/55	0/32	60/140	35/63	12	365	1-3	1
Computers and Peripherals	-40/85	0/55	0/32	60/140	20/36	2	1460	5	0.1
Telecomm	-40/85	-40/85	-40/-40	85/185	35/63	12	365	7-20	0.01
Commercial Aircraft	-40/85	-40/85	-55/-67	95/203	20/36	12	365	20	0.001
Industrial and Automotive - Passenger Compartment	-55/150	-40/85	-55/-67	95/203	20/36 &40/72 &60/108 &80/144	12 12 12 12	185 100 60 20	10-15	0.1
Military (ground and shipboard)	-40/85	-40/85	-55/-67	95/203	40/72 &60/108	12 12	100 265	10-20	0.1
Space leo geo	-40/85	-40/85	-55/-67	95/203	3/5.4 to 100/180	1 12	8760 365	5-30	0.001
Military Aircraft a b c	-55/125	-40/85	-55/-67	125/257	40/72 60/108 80/144	2 2 2	100 100 65	10-20	0.01
Maintenance					&20/36	1	120		
Automotive (under hood)	-55/150	-40/125	-55/-67	125/257	60/108 &100/180 &140/252	1 1 2	1000 300 40	10-15	0.1

& = in addition

1. All categories may be exposed to a process temperature range of 18°C to 260°C [64.4°F to 500°F].
2. Tmin and Tmax are the operational (test) minimum and maximum temperatures, respectively, and do not determine the maximum ΔT.
3. ΔT represents the maximum temperature swing, but does not include power dissipation effects; for power dissipation calculate ΔT; power dissipation can make pure temperature cycling accelerated testing significantly inaccurate. It should be noted that the temperature range, ΔT, is not the difference between Tmin and Tmax ; ΔT is typically significantly less.
4. The dwell time, t_D, is the time available for the creep of the solder joints during each temperature half-cycle.

3.4.3 *Sample Temperature: Ts The temperature of the samples during temperature cycling, as measured by thermocouples, or equivalent temperature measurement apparatus, affixed to, or imbedded in, their bodies. The thermocouple or equivalent temperature measurement apparatus used in the attachment method should ensure that the entire mass of the sample(s) is reaching the temperature extremes and the dwell/soak requirements.

3.4.4 *Maximum Sample Temperature: Ts(max) The maximum measured temperature experienced by the sample(s).

3.4.5 Maximum Nominal Temperature: T(max) The maximum nominal temperature for a specific test condition is the required temperature Ts(max) of the sample; see Table 4-1.

3.4.6 *Minimum Sample Temperature: Ts(min) The minimum measured temperature experienced by the sample(s).

3.4.7 Minimum Nominal Temperature: T(min) The minimum nominal temperature for a specific test condition is the required temperature Ts(min) of the sample; see Table 4-1.

3.4.8 Mean Cyclic Temperature, T_{SJ} The mean of the maximum nominal temperature and the minimum nominal temperature; see Equation 4, Appendix A.

3.4.9 Nominal ΔT The difference between nominal T(max) and nominal T(min) for a specific test condition; see Table 3-1.

3.4.10 Dwell/Soak Time, t_D The total time the sample temperature is within a specified range of each nominal T(max) and T(min) (see Table 4-1). The dwell time is of particular importance for accelerated tests, since during accelerated testing the creep process is substantially incomplete. The dwell allows for a correction of the effect of the incomplete creep process relative to the product use temperature cycles which are typically long enough to allow the creep process to be complete at every cycle dwell.

3.4.11 Dwell/Soak Temperature The temperature that is above T(max) for the upper end of the cycle and is below T(min) for the lower end of the cycle. See Table 4-1.

3.4.12 Cycle Time Time for one complete temperature cycle. See Figure 3-1.

3.4.13 *Temperature Ramp Rate The rate of temperature increase or decrease per unit of time for the sample(s). The temperature ramp rate should be measured for the linear portion of the profile curve, which is generally the range between 10% and 90% of a specific test condition temperature range. Note: Ramp rate can be load dependent and should be verified for the load being tested.

3.4.14 Maximum Cyclic Strain Range The range of total strain experienced during exposure to cyclically induced thermal or mechanical deformations.

3.4.15 Maximum Cyclic Stress Range The range of total stress experienced during exposure to cyclically induced thermal or mechanical deformations. For solder in the temperature range where creep takes place, the stress range and the strain range are independent of each other (this is in contrast to noncreeping metals for which the stress-strain curve defines unique correspondences between stress and strain) since there is a different stress-strain curve for each temperature and strain-rate. The modulus and yield strength are temperature- and strain-rate-dependent, and the maximum stress experienced by the solder joints is strongly dependent on the compliancy of the attached structures, e.g., compliant leads.

3.4.16 Hysteresis Loop This loop diagrams the stress-strain behavior of solder attachments obtained during a loading cycle. The area of the hysteresis loop defines the visco-plastic strain energy per cycle, and is a measure of the fatigue damage per cycle. The size of the hysteresis loop depends on the strain range, stress range, the cyclic dwell time, and to a lesser extent on the mean cyclic temperature.

3.4.17 Design Service Life The required duration of operational life of a piece of equipment that remains fully functional while exposed to the expected environment.

3.4.18 Projected Service Life Service Life predicted by a model using accelerated test results which relates the number of fatigue cycles to a given acceptable cumulative failure probability.

3.4.19 Infant Mortality Failures Failures during environmental stress screening (ESS), burn-in, initial functional testing, and/or early in service occur primarily as a result of inadequate quality and/or manufacturing processes.

3.4.20 Random Steady-State Failures This is a period of useful operation life during which failures occur seemingly at random or at a low rate, weakly related to product complexity. For solder attachments, this period is not measurable because it may not exist or have very low failure rates.

3.4.21 Wearout Failures Wearout is defined as the process where damage accumulates over time and where the occurrences of failures rise steadily as the product deteriorates due to fatigue, or another wear-out mechanism. It is

the wear-out failures due to creep-fatigue of the solder attachments which are the subject of this document.

3.5 Statistical Failure Distribution Concepts

3.5.1 Statistical Failure Distribution Failures, in particular due to wear-out, do not occur all at once, but are distributed over time. The Weibull statistical distribution is the most suitable statistical distribution used for wear-out failures; however, occasionally the Log-Normal distribution is used also. For the Weibull distribution two (2) defining parameters are required: (1) the Weibull slope (a measure of the degree of spread of the distribution), and (2) some intercept value (typically N(63.2%)—the characteristic life of the Weibull distribution, but sometimes N(50%)—the mean fatigue life. On Weibull distribution graph paper, using the two defining parameters, measured data will plot as a straight line, frequently simplifying data analysis.

3.5.2 Mean Fatigue Life, N(50%) The amount of time at which one-half of a given sample has failed.

3.5.3 Failure Free Life, N_0 The amount of time (or number of cycles) prior to the first failure (This parameter is used in a 3-parameter (3-P) Weibull statistical distribution.)

3.5.4 Cumulative Failure Percentage During testing, the cumulative failure percentage of a sample i is calculated by using F (i) = i/(n + 1) where i is the sample ranking.

3.5.5 Cumulative Failure Probability For design purposes the required reliability is typically given as a "Cumulative Failure Probability" not to be exceeded in a given design life.

3.5.6 Acceptable Cumulative Failure Probability The maximum allowable percentage of defectives/failures at the end of the service life.

3.6 Reliability Tests

3.6.1 Accelerated Reliability Test A test in which the damage mechanism(s) of concern for operational use is (are) accelerated to cause failures in less time than in service. The test acceleration results from shorter cycle periods and/or more severe loading conditions; however, the introduction of extraneous damage mechanisms must be avoided. The service life can be estimated by application of appropriate acceleration factors.

3.6.2 Thermal Cycling Exposure of assemblies to cyclic temperature changes where the rate of temperature change is slow enough to avoid thermal shock (typically less than or equal to 20°C [36°F]/min).

The maximum temperature for thermal cycling should be 25°C [45°F] below the glass transition temperature (T_g) of the printed circuit board material.

It must be noted that temperature cycles that extend below -20°C [-4°F] or above 110°C [230°F] or include both cold and hot temperatures (for near-eutectic Sn-Pb solders) may subject the solder attachment to more than one damage mechanism. These mechanisms tend to accelerate each other and thus can lead to earlier failures; furthermore, because of the confounding of multiple damage mechanisms, extrapolation of test results from such environments must be undertaken with a recognition of this fact.

3.6.3 Thermal Shock Thermal shock occurs when an assembly is exposed to rapid changes of temperature causing transient temperature gradients, warpages, and stresses within the part and/or assembly. The rate of temperature change for thermal shock is usually greater than 20°C [36°F]/minute.

3.6.4 Power Cycling Power cycling may more accurately replicate field use conditions than temperature cycle testing for electronic devices that are frequently turned on/off.

3.7 Other Tests

3.7.1 Burn-In Test This test takes finished product and routinely subjects it to normal, perhaps worst-case but still realistic, operational environments. The burn-in test is not an accelerated reliability test.

3.7.2 Environmental Stress Screening (ESS) This screening procedure employs environmentally generated stresses to cause overstressing of "weak" elements of an assembly to the point of failure. It is intended to prevent these latent defects from reaching field service and possibly causing field failures. The environments producing these stresses may or may not be related to environmental conditions experienced by the product during service. Once having failed, the elements can be detected and either repaired, replaced, or discarded, and perhaps redesigned for future product. ESS needs to be accomplished without significant damage to the "normal" elements of the assembly. ESS is not an accelerated reliability test.

3.7.3 Highly Accelerated Stress Testing (HAST) This stress test is used to simulate corrosion related failure mechanisms under electrical bias while being subjected to an accelerated stress combination of temperature and humidity. HAST may be used in the context of components and assemblies, but it is not an accelerated reliability test for solder attachments.

3.7.4 Mechanical Shock Mechanical shock is defined as a rapid transfer of mechanical energy to a system that

results in a significant change in stress, velocity, acceleration, or displacement within a system.

3.7.5 Vibration Vibration in assemblies is defined as periodic or random motion in alternately opposite directions from the position of equilibrium. The application load typically is below the yield point (elastic) of materials.

3.7.6 Process Qualification This is a special test or set of tests which validates a process used to manufacture product that meets performance specifications.

3.7.7 Process Verification A periodic evaluation of a process used to ensure process optimization or eliminate process deviations.

3.8 Evaluation and Application Considerations Table 3-1 shows common storage and operation environments as well as the worst-case use environmental conditions for the nine most common product categories. This table should be used for reference only.

3.9 Understanding of Solder Attachment Technology Solder is unique among engineering metals due to its temperature, time and stress dependent behavior for typical use conditions. For instance, eutectic tin-lead solder readily creeps and stress relaxes above 20°C [68°F], whereas below -20°C [-4°F] solder has long-term load bearing capabilities similar to other metals. The higher the temperature above 20°C [68°F] and/or the higher the stress level, the faster the solder will creep and stress relax.

An understanding of the reliability and failure mechanisms for a given surface mount attachment technology is the first step toward designing and assuring product reliability. For this, a generic database is required. Although failure mechanisms based on monotonic overstressing can occur, the most common reliability threat comes from stress-relaxation based fatigue damage. A desirable fatigue failure database is one that is based upon a combination of low acceleration and high acceleration tests. For near-eutectic Sn-Pb solders such databases exist, however they do not currently exist for other alloys, in particular Pb-free solders.

In this context, low acceleration tests produce mean-times-to-failure of the test vehicles that are about 10 to 20 times shorter than actual life in field use. High acceleration tests are about 100 to 500 times shorter. The higher the test acceleration, the less the test results are representative of performance at field conditions.

Thus, low acceleration tests should closely mimic expected field conditions, whereas high acceleration test are often necessitated by the reality of the time and resources required for the low acceleration testing.

4 PERFORMANCE TEST METHODS

Standardized accelerated reliability test methods are preferred as data results can be correlated to form benchmark reliability bases. IPC-SM-785 provides a technical basis for designing and implementing accelerated reliability testing. The use of this document in conjunction with IPC-SM-785 is highly recommended as this document provides an understanding of the physics of SMT solder joint failure, that is, the various mechanisms which contribute to solder joint fatigue. In addition to formulating failure mechanisms, this document provides technical information based upon empirical studies from which an accelerated test program can be derived. Appropriate caveats and disclaimers are given in IPC-SM-785.

Since the fatigue life of SMT solder joints are far in excess of the usual schedule spans for design and development of electronic boxes, accelerated testing is a necessity for qualification purposes when equipment operational life is a requirement. This document, IPC-9701, provides guidance and methods for devising accelerated life tests for equipment qualification purposes. Although accelerated life tests are frequently agreed to between customer and suppliers, the use of this document, with minor modifications as needed, will lead to standardization for life testing. Consequently, the test methods and requirements contained herein may not be technically rigorous. However, continued usage and the accumulation of data will lead to a reliable database.

4.1 General Requirements Table 4-1 lists both mandated and preferred test parameters. Mandated parameters should be followed without any deviation. Complying with all mandated requirements insures acceptance of the tests and their results by the industry; deviation from a particular mandated parameter may be acceptable to an individual customer but ultimately jeopardizes the acceptance of the supplier's results by the industry. For multiple parameters, preferred reference test parameters are recommended to be used for an even wider-industry compatibility and acceptance. Preferred parameters should be followed unless the supplier can substantiate that their proposed deviation is expected to enhance board-level reliability of the specific package.

4.2 Test Vehicles Proper design and assembly of the test vehicles (TVs) are critical to assure that valid and appropriate data are obtained.

4.2.1 Component Description This document assumes a surface mount (SMT) component to be one that is attached onto a circuit board with a solder alloy using conventional reflow technologies. Ball Grid Array (BGA), Small Outline Package (SOP) and Chip Scale Package (CSP) are some typical component examples.

Table 4-1 Temperature Cycling Requirements, Mandated and Preferred Test Parameters Within Mandated Conditions

Test Condition	Mandated Condition
Cycle (TC) Condition: *TC1* TC2 TC3 TC4 TC5	 *0°C ⟷ +100°C (Preferred Reference)* -25°C ⟷ +100°C -40°C ⟷ +125°C -55°C ⟷ +125°C -55°C ⟷ 100°
Test Duration Number of Thermal Cycle (NTC) Requirement: NTC-A NTC-B NTC-C NTC-D *NTC-E*	Whichever condition occurs FIRST: 50% *(Preferred 63.2%)* cumulative failure (Preferred Reference Test Duration) or 200 cycles 500 cycles 1,000 cycles (Preferred for TC2, TC3,and TC4) 3,000 cycles *6,000 cycles (Preferred Reference TC1)*
Low Temperature Dwell Temperature Tolerance (preferred)	10 minutes +0/-10°C (+0/-5°C) [+0/-18°F (+0/-9°F)]
High Temperature Dwell Temperature Tolerance (preferred)	10 minutes +10/-0°C (+5/-0°C) [+18/-0°F(+9/-0°F)]
Temperature Ramp Rate	≤20°C [36°F]/minute
Full Production Sample Size	33 component samples (32 test samples plus one for cross-section, add additional 10 samples for rework, if applicable)
Printed Wiring (Circuit) Board (PWB/PCB) Thickness	2.35 mm [0.093 in]
Package/Die Condition	Daisy-Chain Die/Package (see Table 4-2)
Test Monitoring	Continuous Monitoring (see Table 4-4, Preferred Reference-Event Detector)

This qualification and requirements standard will address solder joint reliability and the thermomechanical component/board interactions while other board level thermal cycling interactions, i.e., delaminations, via cracks, dielectric cracks, etc., are more appropriately addressed in component qualification standards.

The default condition of this standard mandates the use of a daisy-chain die to assure that the reliability of solder balls, package materials, and die-level interconnect are all characterized during board-level temperature cycling. Exemptions to the daisy-chain die requirement are listed in Table 4-2. Specific parameters on the exemption are given in Table 4-3. Mechanical die, when permitted, should replicate an actual die with regard to dimensions and die-level interconnect but are required to include daisy-chain pairs or active silicon circuitry.

Table 4-2 Daisy Chain Requirements

Exemption Category	Mandated Condition
Full Product Characterization (Default)	Daisy-Chain Die
Exemption Category A (see Table 4-3)	Daisy-Chain Package Substrate & Mechanical Die (Preferred Daisy-Chain Die)
Ceramic Package (Substrate >1 mm [0.040 in] thick with an average modulus of 240-270 GPa)	Daisy-Chain Package Substrate (Preferred Daisy-Chain)

4.2.1.1 Daisy-Chain Die/Package The TV component package and die should be representative of the production component. This means:

1. The TV component layout, construction and materials are mandated to be representative of a typical production component, including the die attach adhesive and process, underfill and process, wire bond/flip chip, etc.

2. The die for the TV component is daisy-chained when applicable (see Table 4-2). The test device must use package materials and dimensions representative of production components, and must connect to the external leads/balls/pads using the same die interconnects, trace geometries, via constructions, layer counts, etc., as in the production component. To reduce further test expenses, the daisy-chain die should match the maximum die size anticipated for the component in production use.

For plastic BGA/CSP, the solder balls underneath the die are often the first to fail in board-level temperature cycling; consequently, daisy-chain coverage of this region must be included, even if the solder balls are exclusively ground and/or power. For ceramic components, corner balls fail early and should be considered critical. Daisy-chain coverage for power/ground solder balls distributed within a peripheral BGA/CSP solder ball matrix are not required;

Table 4-3 Test Exemption Requirements –
A: Use of mechanical die rather than daisy-chain PQ 9701, previously qualified per IPC 9701

If [New] device does not meet requirements listed below for exempt A Category, then the default Full Product Characterization applies.		
Description	**EXEMPT**	**Exemption Category A**
Package body size	[NEW] ≤110% [PQ 9701]	[NEW] ≤120% [PQ 9701]
Die* dimensions	[NEW] ≤110% [PQ 9701]	[NEW] ≤120% [PQ 9701]
Solder ball diameter, if applicable	[NEW] ≥90% [PQ 9701]	[NEW] ≥80% [PQ 9701]
Wetted solder pad diameter, if applicable	[NEW] ≥90% [PQ 9701]	[NEW] ≥80% [PQ 9701]
Solder ball pitch or lead pitch	[NEW] ≥90% [PQ 9701]	[NEW] ≥80% [PQ 9701]
Solder ball stand-off or lead stand-off	[NEW] ≥90% [PQ 9701]	[NEW] ≥80% [PQ 9701]
Substrate thickness	[NEW] = [PQ 9701] ± 20%	[NEW] = [PQ 9701] ± 40%
Stiffener and/or heat spreader dimensions, if applicable	[NEW] = [PQ 9701] ± 20%	[NEW] = [PQ 9701] ± 40%
Epoxy/encapsulant dimensions	[NEW] = [PQ 9701] ± 20%	[NEW] = [PQ 9701] ± 40%
Die attach* dimensions, if applicable	[NEW] = [PQ 9701] ± 20%	[NEW] = [PQ 9701] ± 40%
Underfill* material dimensions, if applicable	[NEW] = [PQ 9701] ± 20%	[NEW] = [PQ 9701] ± 40%
Organic material critical properties (modulus, CTE, ultimate strength, etc.)	[NEW] = [PQ 9701] ± 20%	[NEW] = [PQ 9701] ± 20%
Organic material suppliers (substrate, die attach*, mold epoxy, encapsulant, underfill*, etc.)	[NEW] = [PQ 9701]	[NEW] = [PQ 9701]
Lead material composition and lead base metallization	[NEW] = [PQ 9701]	[NEW] = [PQ 9701]
Stiffener and/or heat spreader materials, if applicable	[NEW] = [PQ 9701]	[NEW] = [PQ 9701]
Solder ball land pad type (SMD, NSMD, etc), if applicable	[NEW] = [PQ 9701]	[NEW] = [PQ 9701]
Ball array layouts (full matrix vs. depopulated), if applicable	[NEW] = [PQ 9701]	[NEW] = [PQ 9701]
Numerical/analytical modeling completed for [NEW] device **	Mandated	Preferred

* Not applicable for ceramic substrates ≥1 mm thick with an average modulus in the range of 240 to 270 GPa and with no lid attached.
** Analytical techniques must be validated by comparison of predictions to experimentally obtained solder joint reliability data for [PQ9701] device. Critical property data (modulus, CTE, ultimate strength, etc.) for organic materials must be experimentally obtained.
[NEW] = New device
[PQ 9701] = Device that test data complied with Full Product Characterization requirements of IPC-9701

however, dasiy-chain stitch patterns must provide some level of coverage for all device rows and/or critical regions.

Designs in which a single continuous daisy chain is monitored for each package will be considered acceptable. It is, however, preferable that multiple nets be monitored independently on each part, and that these nets be designed to provide additional information on the region(s) of first failure.

An example for a BGA/CSP, using four - five nets per package might include isolation of failures as follows:

(a) The package corner solder attachments.

(b) The outer rows of solder attachments.

(c) Solder attachments under or nearly under the die perimeter.

(d) Central package solder attachments, if present.

For Daisy-Chain Net, the known high failure risk regions should be on separate daisy-chain nets than those of known low failure locations.

4.2.1.2 Solder Ball Shear Test Perform solder ball shear test, if applicable. The minimum shear force is defined as the mean minus 3 sigma, for a minimum of three packages, 10 solder balls each. Perform shear by applying a force against the edge of the BGA/CSP parallel to the plane of the substrate. The height of shearing tool should make a gap with the chip surface of 50 μm [0.002 in] minimum. Shear test at nominal speed of 500 μm/sec [0.020 in/sec] is preferred. The failure mode for the sheared balls **shall** be either bulk solder failure or copper pad lift-off, an intermetallic failure is unacceptable. Shear testing at much higher speed is recommended to determine the effect of shear speed on shear strength and failure mechanisms. See JESD22-B117 BGA Ball Shear Test.

4.2.1.3 Component Documentation Requirements The following covers all requirements for component documentation:

1. Package outline drawing or reference to JEDEC[6] outline.
2. Internal die dimensions (LxWxH) and orientation (if die is not square).
3. Package daisy-chain connection map and/or net list (electronic files preferred).
4. Measured solder ball/lead coplanarity (seating plane method or best fit place).

6. www.jedec.org

5. Solder ball shear values or lead pull test, if applicable, and failure modes for parts from same production lot as tested devices. Pull test is optional.
6. Measured x and y CTE by micro-Moiré interferometry data, preferred for area array packages, for parts from same production lot as tested devices. Other techniques such as TMA are also acceptable where appropriate for the determination of effective CTEs.
7. Solder-wetted pad dimensions, if applicable.
8. Solder ball land pad type, if applicable (solder mask defined (SMD) with coverage of mask on pad, non-solder mask defined (NSMD) with a gap between mask and pad, or via-in-pad).
9. Lead finish/pad metallization construction, including thicknesses of all layers and composition of solder, if applicable.
10. Illustration showing daisy-chain interconnection path, if applicable, from die to lead.
11. Die-to-lead interconnection table (electronic file preferred).

4.2.2 Printed Wiring (Circuit) Boards PWB/PCB lay-up, thickness, and pad design can affect solder attachment integrity. The nominal mandated reference PWB thickness **shall** be 2.35 mm [0.093 in] (see Table 4-1). Two PWB thicknesses are preferred to be used for the first qualification of a package family to aid analytical extrapolation of empirical test results for application. The additional PWB thickness may vary and can have thickness values lower and/or higher depending on the user application.

In addition to the PWB TV layer construction recommended below, it is important to design with an even number of layers, resulting in a symmetrical cross section. This symmetry also applies to signal layers. This is necessary since copper and epoxy/glass have different coefficients of thermal expansion and the PWB would warp during processing if not symmetrical.

It is recommended that standard PWB design methodology be used to design the daisy-chain test boards. This should include defining the package(s) to be tested in a component library along with any connectors (if they are used), incorporating the daisy-chain interconnectivity for all packages used into the component definitions, and by creating an actual schematic for the test board. By doing this the test board can be designed using the standard design flow methodology which is used for a product PWB.

This design flow typically includes both interactive tools and design checks which insure that all nets are connected. Doing the above greatly increases the odds of a good first time PWB TV design. Conversely, assuming that this is a "simple" test board and designing on a CAD system that does not check for the correct electrical connection of all parts greatly increases the odds of failure.

4.2.2.1 Test Board Design Requirements The following include all requirements necessary for test board design:

1. For PWBs, preference is given to the 2.35 mm [0.093 in] thick PWBs with a minimum of six copper layers; for thicker or thinner PWBs, the number of layers should be proportionally increased or decreased, respectively.
2. For package body sizes larger than 40 mm [1.57 in], the use of 3.15 mm [0.125 in] thick PWB with a minimum of eight copper layers is preferred.
3. The PWB TV is preferred to have the same material and layup as the product PWB; however in all cases the measurement of the glass transition temperature, T_g, as well as the CTE in both x and y planar directions is mandated.
4. Representative power/ground planes in even internal layers (total PWB layer count is even) is mandated to have nominal 70% Cu coverage.
5. Representative signal traces in odd internal layers (total PWB layer count is even) is mandated to have nominal 40% Cu coverage.
6. Daisy-chain nets are preferred to be in outer layers only.
7. The trace routing is preferred to be isolated such that a device can be cut away w/o compromising other devices on the board. Additional reference traces should be placed by design close to pads to be used only during solder paste height measurement by automatic visual systems such as a 3D laser. These traces are needed since the visual system requires a reference to pad surface which is covered by solder paste.
8. Although daisy-chain nets will typically not require PWB TV vias, the PWB TV is mandated to contain vias at a minimum of 50% of the land pad sites to approximate mechanical effect of vias on product PWBs.
9. OSP (Organic Solderability Preservative) surface finish is preferred. HASL (Hot Air Solder Levelling) is optional.
10. NSMD (Non-Solder Mask Defined) is mandated if applicable.
11. The PWB pad diameter for solder ball attachment is preferred to be 80% - 100% of the component solder-wetted pad diameter.
12. Multiple probe pads are required for each daisy chain net to ease failure analysis.
13. Nominal outer layer copper thickness is preferred to be 35 µm [137.8 µin].
14. Minimum outer layer trace width is preferred to be 150 µm [590.6 µin].

15. Minimum of 5 mm [0.2 in] clearance, plus routing space for failed package removal, if applicable, between package body and adjacent packages, connectors or board edge is required.
16. For solder mask registration, no overlap on surface mount pads is allowed. No solder mask allowed on NSMD pads.
17. For board warpage, it is required that the PWB warpage is within the values defined by industry standards such as IPC-2221, IPC-6012 and IPC-A-600. These standards refer to PWB warpage as "bow and twist."
18. Components anticipated for use in mirror-sided (dual-sided) board assemblies are mandated to be tested in a mirror-sided board configuration.
19. Silkscreen nomenclature or Cu etch, including but not limited to, legends which clearly label all components on the test board and all test points, and location of pin 1 for correct package on board assemly, is mandated for ease in assembly, ATC and FA.

4.2.2.2 Test Board, Daisy-Chain Design The combination of daisy-chain links on the component and those on the PWB TV should result in a completed daisy-chain net after assembly. It is preferred that the daisy-chain trace-links be placed on the top PWB layer, wherever possible. This is to avoid missinterpretation of daisy-chain failures due to via failure. It is highly recommended that accelerated testing be performed on bare PWB prior to assembly to assure quality and to minimize the likelihood of via failure during board-level testing.

It is mandated that component/PWB daisy-chains be monitored continuously. However, it is preferred that multiple manual probe pads be located within each daisy-chain net to ease fault isolation. The use of multiple jumper locations within each daisy-chain net can enable continued testing of the device for additional failure locations.

4.2.2.3 Test Board Documentation Requirements The following cover all requirements for documentation of test boards:

1. PWB Lay-Up.
2. Dielectric material.
3. Internal trace, plane and via geometries, preferred.
4. External geometries.
5. Plating finish.
6. Measured x/y-CTE (coefficient of thermal expansion), TMA or Moiré interferometry, preferred.
7. Measured glass transition temperature, T_g.
8. Test board orientation in thermal chamber.

4.2.3 Board Assembly For many applications, SMT devices are assembled onto circuit boards using not only mass-reflow conveyor furnaces, but also using hot gas rework stations. Consequently, it is preferred that daisy-chain devices are assembled onto the test boards using both reflow methods. The term rework applies to the reflow operation using rework equipment and not to the re-use of any devices. The devices for rework **shall** be virgin, identical to the mass-reflow assembled devices.

Moisture absorption of the daisy-chain components prior to either the mass reflow or rework assembly process could result in delamination at various package interfaces. Several studies have also demonstrated that a multiplicity of board assembly parameters affect not only the yield, but the reliability of solder attachments. Consequently, it is critical that the documentation accompanying solder attachment reliability test results include the test board assembly documentation listed below.

An adhesively or mechanically attached heatsink can affect solder attachment reliability and may need to be evaluated in application-specific testing, separate from this standard.

4.2.3.1 Board Assembly Requirements Board Assembly Location Process parameters must be optimized prior to assembly. Optimization process parameter examples include solder volume, paste registration, printing speed, squeegee pressure, stencil snap off, thermal profile, etc.

Component Bake-Out Prior to Board Assembly Production storage/bake-out procedures, if available, should be used.

If a qualified moisture resistance level or bake-out specification is not finalized for the device, then a default bake-out of 24 hours at 125°C [257°F] is required.

Board Assembly Bake-Out Prior to Rework Processing Production storage/bake-out procedures, if available, should be used.

If a qualified moisture resistance level or bake-out specification is not finalized for the PWB, then a default board bake-out of 24 hours at 105°C [221°F] is required.

Assembly Inspection X-Ray of all solder attachments **shall** be performed after assembly to identify solder attachment defects. Defects to be identified include: solder bridge, solder open, missing solder contacts, large number of voids, solder ball misalignment and lack of fillets. Assemblies with gross defects must not be included in reliability evaluation. Manufacturing processes optimization is recommended to be repeated if multiple gross defects are detected.

All assemblies must be tested for electrical continuity. Any open, short, or abnormality in initial daisy-chain resistance is not acceptable. Samples with any open, short, and/or abnormality in initial resistance should not be monitored in ATC.

4.2.3.2 Test Board Assembly Documentation The following represent the requirements for proper documentation of the test board assembly:

1. Reflow temperature characterization including pre-heat temperature, ramp rate, critical peak temperatures (solder, package surface, board, etc.), duration above solder liquidus temperature and cooling rate. Include reflow atmosphere and thermocouple locations and attachment configurations.
2. Solder composition and solder paste metal percentage, particle mesh size and flux type.
3. Nominal solder paste volume.
4. Nominal solder attachment standoff.
5. Nominal ball diameter or fillet shape, preferably by diagonal cross-section and/or x-ray laminography.
6. Number of rework operations completed (default = one) at each test board rework site.

4.3 Accelerated Temperature Test Methods

4.3.1 Preconditioning by Isothermal Aging Select non-commercial customers prefer that test vehicles, following board assembly, should be subjected to an accelerated thermal aging (e.g., 24 hours at 100°C [212°F] {(-0/+5°C), (-0/+9°F)}) in air to simulate a reasonable use period and to accelerate such possible processes as solder grain growth, intermetallic compound growth, and oxidation. Storing the test vehicles after this artificial aging for some additional time at room temperature before commencing with the fatigue testing serves to further stabilize the solder structure.

4.3.2 Temperature Cycling Note: Paragraphs denoted with an asterisk (*) are reprints of text taken from JESD22-A104-B.

4.3.2.1 *Temperature Chambers The chamber(s) used **shall** be capable of providing and controlling the specified temperatures and cycle timing in the working zone(s), when the chamber is loaded with a maximum load. Direct heat conduction to sample(s) **shall** be minimized. The capability of each chamber achieving the sample temperature requirements **shall** be verified across each chamber by one or both of the following methods:

(a) Periodic calibration using instrumented parts and a maximum load, and continual monitoring during each test of such fixed tool thermocouple temperature measurement(s) as adequate to ensure run-to-run repeatability.

(b) Continual monitoring during each test of an instrumented part or parts placed at worst-case temperature locations (for example, this may be the corners and middle of the load).

4.3.2.2 *Test Procedure Sample(s) **shall** be placed in a position with respect to the air stream such that there is substantially no obstruction to the flow of air across and around each sample(s). When special mounting is required, it **shall** be specified. The sample **shall** then be subjected to the specified temperature cycling test condition for the specified number of cycles. Completion of the total number of cycles specified for the test may be interrupted for test chamber loading or unloading of device lots, manual verification of interruptions or as the result of power or equipment failure. However, the number of interruptions **shall** be minimized. If the thermocouple is affixed to the sample body, the amount of glue or tape used **shall** be minimized to insure proper temperature measurements. The thermocouple, or equivalent temperature measurement apparatus, attachment method used should ensure that the entire mass of the sample(s) reaches the temperature extremes and the dwell/soak requirements.

When testing interconnections for solder joint fatigue, it is important to avoid transient thermal gradients in the samples on test. Samples with large thermal mass and low heat transfer efficiency require ramp rates slow enough to compensate for the thermal mass. The temperature of the sample should be within a few degrees of the chamber ambient temperature during the temperature ramps. For samples of large thermal mass, use of a single zone chamber may be required to achieve the mandated ramp rate.

The following conditions are mandated or preferred as described below:

a) Preferred single zone chamber with air in which assembled boards are vertically oriented and are parallel to air flow are preferred.

b) Board temperature measurements preferred to be made at six boards at different chamber locations, two within the center area of the chamber and four toward the perimeter.

c) Dwell time at each end of the temperature limit, heat up and cool down rates (ramp rates) as listed in Table 4-1. Use the average of thermocouples on boards for the ramp rates calculation. Ramp rate should be measured between the maximum low temperature soak limit, and the minimum high temperature soak limit.

4.3.3 Test Monitoring

4.3.3.1 Temperature Monitoring The temperature monitoring requirements are given in Table 4-4.

4.3.3.2 Electrical Daisy-Chain Monitoring The electrical daisy-chain monitoring requirements are given in Table 4-4. Continuous electrical monitoring mandated to be performed by an event detector and/or data logger, though the event detector technique is the preferred reference test. Manual read points are not an acceptable alternative to continuous monitoring.

Table 4-4 Test Monitoring Requirements

Test Parameter	Mandated Condition
Temperature (Chamber Characterization)	Component temperature to be monitored and recorded at each board location in chamber during initial chamber set-up. Characterization study should be performed using representative sample loads, test board configurations and fixturing.
Temperature (Chamber Test Operation)	Continuous component temperature monitoring of at least two devices, total, on two test boards (chamber center and perimeter), as well as chamber ambient.
Electrical (High and Low Temperatures)	Continuous intermittent event monitoring (preferred reference) OR Continuous electrical resistance monitoring (maximum scan interval of all chains = one minute). Manual monitoring is not allowed.
Failure Definition	Event detector: 1000 Ω, 10 events (maximum), 1 micro-second duration (maximum), report first verified as time-to-failure AND/OR Data logger/Voltmeter: 20% nominal resistance increase (maximum), five readings/ scans (maximum)

Solder joint fractures almost always electrically manifest themselves as very short-duration opens or high-resistance connections. The primary advantage in an event detector is the ability to capture these intermittent high-resistance events, which typically precede a measurable resistance increase, shortly after the full fracture of a solder joint occurs. The most significant disadvantages of an event detector are false failure indications due to minor electrical noise in the test apparatus, cabling and/or connectors. A data logger detects and records resistance changes. Using a data logger to scan interval durations of less than one minute is mandated. Regardless of the continuous monitoring method, manual verification is required to reduce the likelihood of false failures due to associated cabling, connectors, PWB TV or test apparatus problems.

Manual monitoring at thermal cycling intervals are not an acceptable alternative to continuous monitoring. Not only does manual monitoring ignore initial failures at high/low temperatures, but the accuracy of the failure durations are dependent on the manual sampling frequency. Further, this method disturbs the tests, is uncertain finding failures when they occur, and is very time consuming.

4.3.3.3 Failure Definition Failure is defined for the event detector as the first interruption for a period of one microsecond or less and increase in daisy chain resistance to 1,000 Ω or more, and affirmation of the failure by nine or more additional events within 10% of the cycles to initial failure. Large numbers of interruptions are required to be monitored in order to assure that failures are due to interconnections. Interruption events associated with noninterconnect failure such as apparatus/software malfunctions **shall** be documented.

For the data loggers, failure is defined as a maximum of 20% nominal resistance increase within a maximum of five consecutive reading scans.

The failure definitions are given in Table 4-4.

5 QUALIFICATION REQUIREMENTS

5.1 Thermal Cycling Ranges The thermal cycling requirements are given in Table 4-1. The thermal cycling requirement for any product should be determined by the user or customer to meet specific environmental operational conditions of the product. Preferred reference should be given to temperature cycle condition TC1 (0°C [32°F] to 100°C [212°F]) and test duration NTC-E (6,000 cycles) for acceptance of test results by a wider industry sector.

The thermal cycling requirements are given in Table 4-1.

Four Test Condition temperature cycling ranges and their allowable temperature tolerances are defined in Table 4-1. Except for the tolerances, Test Conditions TC1, TC3, and TC4 are the same as test conditions J, G, and B in JEDEC 22 Method A 104 Revision A, respectively.

***CAUTION:** Care should be taken when selecting Test Conditions, since: 1) the T(max) requirement for a specific Test Condition may exceed the glass transition temperature region (T_g minus 25°C [45°F]) of the PWB which would cause a significant change in the physical properties of the PWB and induce a nonlinear change in the loading conditions, 2) the T(max) requirement for a specific Test Condition may exceed the glass transition temperature of some component materials which may induce failure mechanisms not normally seen during design application conditions in the field, and 3) CTE differences over the test condition temperature range can produce premature failure of plated-through holes in the test board, thus limiting electrical readout capability for the parts being tested.

Additional disadvantages of the Test Conditions TC3 and TC4 are:

1) Reduced compatability with high aspect ratio vias on test boards.

2) Reduced correlation of modeled and measured material characteristics over the wider temperature range.
3) Reduced accuracy of extrapolated lifetimes given the relatively benign actual-use temperature ranges of most electronic applications.

5.2 Thermal Cycling Test Durations The thermal cycling test duration requirements for any product should be determined by the user or customer to meet specific environmental operational conditions of the product. The thermal cycling test duration requirements are given in Table 4-1. Preference should be given to temperature cycle condition TC1 (0 to 100°C [32°F to 212°F]) and test duration NTC-E (6,000 cycles). Testing to 63% failures is always performed to characterize the failure distribution.

***CAUTION:** Care should be taken when extrapolating accelerated test results for the product life-cycle in operational use. The short dwell/soak times at the temperature extremes results in incomplete creep process. Thus, even though the applied strain and stress ranges may be larger for accelerated test than during operational use, the cyclic hysteresis loops for test could be smaller. The test acceleration is primarily one of shorter mean-time-to-failure and not necessarily one of less cycles-to-failure.

When 50% (preferred 63.2%) cumulative failure of samples occur prior to defined NTC levels, then the test duration is defined by the number-of-cycles to the failure of the last failed samples.

5.3 Number of Samples A total of 33 components is mandated for Default Product Characterization (see Table 4-1). Of these, 32 are to be tested, and one sample is to be cross-sectioned after assembly. Use of a minimum of 10 additional virgin samples for rework assembly and its effects on reliability is strongly recommended for Full Default Characterization.

For Category A Exemption (see Table 4-3), additional samples for rework test are not required.

5.4 Test Exemption Requirements The conditions that have to be met to obtain a test exception are listed in Table 4-3 under Exempt column. No testing is required when the [New] device meets, with history of full Default Protection characterization per IPC-9701, meets the Exempt requirements specified in this column.

6 FAILURE ANALYSIS

The obvious goal of failure analysis is the ability to detect the location, mode, and mechanism for the observed electrical failure. In many cases, it is not readily obvious if the failure is within the test cable/connector, test board, solder attachment or internal package interconnect. Thoughtful design of the test board, daisy-chain die and overall interconnect scheme can help to reduce the effort of failure isolation.

6.1 Failure Analysis Procedures Common failure analysis methods include optical and scanning electron microscopy (SEM), X-ray and coupled scanning acoustic microscopy (CSAM), cross section (transverse and parallel), and dye-and-pry (pressurized dye exposure of assembled unit followed by mechanical package removal). After nondestructive characterization of failures, it is preferable to perform both cross-sectioning and dye-and-pry evaluation.

For tests stopped at the end of an NTC level with ZERO failure, the supplier must perform failure analysis (three randomly selected devices, minimum, per board test type) to insure that failures were not missed due to errors in daisy-chain design or test hardware.

6.2 Data and Failure Analysis Documentation Requirements The following documentation requirements are mandated:

1. Detailed description of all experimental apparatus, including thermal chamber and data acquisition systems.
2. Temperature vs. time plots for both boards and chamber (chamber set-up characterization data).
3. Resistance vs. time plots for data logger samples.
4. Tabular data for number of cycles to failure for all failures, electronic file(s) preferred.
5. 2-Parameter Weibull plots for all failures, preferred.
6. Failure analysis samples and identification of failure modes (dye-and-pry, CSAM, cross-section, X-ray or whatever characterization technique is appropriate) and root cause identification of three samples, minimum, per test board type and major failure mode.
7. For tests stopped at NTC level with ZERO test failures, failure analysis documentation of three randomly selected devices, minimum, per test board type.
8. Time-zero diagonal cross-section of single, representative package/board assembly.

7 QUALITY ASSURANCE

7.1 Responsibility for Inspection Unless otherwise specified in the contract, the supplier is responsible for the performance of all inspection requirements to assure quality conformance to inspection requirements specified in this document. The user reserves the right to perform any of the inspections set forth in the specification where such inspections are deemed necessary to assure supplies and services conform to prescribed requirements.

7.2 Quality Conformance Inspection

7.2.1 As Assembled Inspection Inspection for solder joint gross defects **shall** be performed by nondestructive X-ray technique on assemblies as specified in 4.2.3.1. The nondestructive inspection along with the cross-sectioning

sample inspection specified in 5.3 **shall** be used to determine the presence of assembly gross defects. If the gross defects reflect a non-optimized assembly process, then new assemblies **shall** be fabricated after inspection of components and PWBs to assure conformance to their general requirements specified in 4.2.2 and 4.2.3 and further assembly process optimization. Key inspection parameters are:

1. **Component** Inspection of component coplanarity to meet JEDEC requirements. Review recommended component bake out and assure compliance.
2. **PWB** Inspection of PWB warpage to meet IPC requirements. Visual inspection of solder mask misregistration and documentation of mask coverage on pad. Mask coverage is not allowed.
3. **Assembly** Inspection of solder paste type and expiration, squeegee blade, stencil, solder paste consistency on PWB, and package placement. Solder paste is required to cover all pads. Inspect reflow profile and assure to meet manufacturing practice.

7.2.2 Thermal Cycling Inspection Inspection **shall** be performed on at least three samples of thermal profiles generated by thermocouples at three thermal cycling intervals, start, middle, and completion; to assure they meet the thermal cycling condition requirements specified in Section 5.

7.2.3 Failure Analysis Inspection Failure analysis **shall** be performed as specified in section 6.1. For the test stopped at the end of an NTC level with ZERO failure, cross-sectional and dye-and-pry samples **shall** be used for mapping to assure that zero failure condition is met.

APPENDIX A

A.1 ACCELERATION FACTORS

Analytical and computational models have not been fully established to replace empirical solder joint reliability evaluation. The solder joint reliability modeling to estimate acceleration factors can be simple to complex depending on experience and resources available. Nonetheless, component end-users increasingly leverage both empirical and computational solder joint reliability studies to estimate actual field-use lifetimes. It is recommended that the suppliers responsible for the design and material selection of package provide mechanical models and material property tables for the empirically tested device.

There are two acceleration factors that need to be considered: AF(cycles), which relates the cyclic fatigue life of solder joints obtained in a test to the life of a product in a given use environment; and AF(MTTF), which relates the time to failure of solder joints obtained in a test to the life of a product in a given use environment. The acceleration factor in terms of cycles to failure is

$$AF(cycles) = \frac{N_f(product)}{N_f(test)}$$

(Eq. 1)

where N_f(product) is the mean fatigue life, N_f (50%), of the product in service and N_f(test) is the mean fatigue life, N_f (50%), of the test vehicles simulating the product in testing. The acceleration factor in terms of time to failure is

$$AF(MTTF) = AF(cycles) \times \frac{f(test)}{f(product)}$$

(Eq. 2)

where f(test) is the test cycle frequency and f(product) is the cyclic frequency in service.

A.2 AN EXAMPLE OF ACCELERATION FACTOR CALCULATION

The following is one example of such calculation provided to compare the effects of key variables and should be used as reference only. Similar acceleration factor calculations resulting from other models will be included as they become available.

The acceleration factors given below are based on the Engelmaier-Wild model given in IPC-D-279, Appendix A-3.1. It needs to be noted, that the temperature cycling ranges for test conditions TC3, and TC4 violate the stated caveats for the underlying model; these caveats are a consequence of the time-, temperature-, and stress-dependent material behavior of solder.

In the Engelmaier-Wild model the fatigue ductility exponent, m, given below accounts for the incomplete creep/stress relaxation process within solder joints during accelerated testing. It accounts for the faster creep rates at higher temperatures (T_{SJ}, in °C) and the more complete creep for longer cyclic dwell times (t_D=half-cycle dwell time in minutes).

$$\frac{1}{m} = 0.442 + 6x10^{-4} \bullet T_{SJ} - 1.74x10^{-2} \bullet \ell n\left(1 + \frac{360\ minutes}{t_D}\right)$$

(Eq. 3)

The mean cyclic solder joint temperature, T_{SJ}, is given in the equation below.

$$T_{SJ} = \frac{1}{4}\,[T(max,comp.) + T(max,sub.) + T(min,comp.) + T(min,sub.)]$$

(Eq. 4)

In Table A-1, values for m are given for the four (4) test levels and some typical product temperature cycles.

For the different test conditions the values of m are different because T_{SJ} is different for each of the test levels; for the typical product cycles the values of m are the same because in all cases T_{SJ} = 30°C [54°F] and t_D = 660 minutes.

In Table A-2, values for the mean fatigue lives, N_f (50%), for a given component with fixed design parameters are given for the four (4) test levels and the four (4) typical product cycles given in Table A-1, based on the solder attachment fatigue model in IPC-D-279, Appendix A. Also given are the values of AF(N) and the acceleration factors in terms of mean time to failure.

It should be noted, that the values of N_f and AF are all for identical components on identical PCBs and the differences in life are solely the result of the differences in test and product service conditions.

Table A-1 Values for Exponent "m" for the Four Test Condition Levels and for Four Representative Product Use Conditions

Test Condition					Typical Product Cycles			
Test	ΔT	T(min)	T(max)	m	ΔT	T(min)	T(max)	m
TC 1	100°C [180°F]	0°C [32°F]	+100°C [212°F]	2.444	20°C [36°F]	+20°C [68°F]	+40°C [104°F]	2.210
TC 2	125°C [225°F]	-25°C [-13°F]	+100°C [212°F]	2.490	60°C [108°F]	0°C [32°F]	+60°C [140°F]	2.210
TC 3	165°C [297°F]	-40°C [-40°F]	+125°C [257°F]	2.471	100°C [180°F]	-20°C [-4°F]	+80°C [176°F]	2.210
TC 4	180°C [324°F]	-55°C [-67°F]	+125°C [257°F]	2.499	140°C [252°F]	-40°C [-40°F]	+100°C [212°F]	2.210

Table A-2 Mean Fatigue Lives for a Given Component Assembly for the Four Test Condition Levels and for Four Representative Product Use Conditions, and Their Respective Acceleration Factors

Test Condition			Typical Product Cycles			
Test	ΔT	$N_f(50\%)$ $N_f(1\%)$	ΔT	$N_f(50\%)$ $N_f(1\%)$	AF(N)	AF(MTTF)
TC1	100°C [180°F]	17,100 5,910	20°C [36°F]	221,000 76,700	12.9	310.2
TC2	125°C [225°F]	11,900 4,140	60°C [108°F]	19,500 6,770	1.63	39.2
TC3	165°C [297°F]	5,570 1,930	100°C [180°F]	6,300 2,190	1.13	27.2
TC4	180°C [324°F]	4,980 1,730	140°C [252°F]	3,000 1,040	0.60	14.4

APPENDIX B
Guidelines for Thermal Cycle Requirements for Pb-Free Solder Joints

B.1 PURPOSE

The following *guidelines* provide additional recommendations to the indicated sections of IPC-9701 for testing Pb-free solder joints. Recommendations for changes in the thermal cycle profile given here are based on current industry understanding and test results as of the publication of this document. Data of the impact of various thermal cycle profiles on the results of accelerated testing in comparison to eutectic tin-lead solder continue to be gathered by industry.

Currently, there is only limited data and insight in determining acceleration factors and acceleration models for Pb-free solders [B1-B14]. The results of the test method, in conjunction with an accelerated test factor different for each Pb-free solder, may in the future provide the ability to estimate product reliability.

B.2 APPLICABLE DOCUMENTS FOR Pb-FREE SOLDER ALLOYS

IPC/JEDEC-J-STD-020 Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Device

B.3 GUIDELINES FOR Pb-FREE SOLDER JOINTS

The following sections provide additional recommendations to existing IPC-9701 section requirements when utilizing a Pb-free soldering process.

B.3.1 Recommendations to 2.2, Joint Industry Standard The most recent IPC/JEDEC J-STD-020 specification should be used for the Sn-Ag-Cu (SAC) system. This specification, in conjunction with component manufacturer recommendations for moisture and bake out prior to solder reflow, should be considered to ensure that test vehicles are not damaged by the manufacturing process.

B.3.2 Recommendations to 3.3.3, Solder Creep-Fatigue Model There is no comprehensive model, available at the time of publication for this appendix, for Pb-free solder creep-fatigue similar to that provided in Appendix A; however, there are currently a number of models for SAC alloys, but none for tin-bismuth (Sn-Bi) solder alloys. Examples of such models for thermal cycling reliability are given in references [B1-B10]. Note that most of these models are undergoing further validation by model developers and end users.

The models can be categorized as analytical [B4, B6, B7], one-dimensional strain-energy based [B2] or finite-element strain-energy based models [B1, B3, B5, B8, B9, B10]. Because of the empirical correlation of the models to generally unrelated failure datasets (including different types of packages, board assemblies, thermal conditions and failure criteria), end users should assess for themselves the most appropriate models for a particular design and use conditions of interest. When fully validated models become available, they will be included in an updated version of this appendix.

B.3.3 Recommendations to Table 4-1, Accelerated Thermal Cycle Profile For Tin-Silver-Copper (SAC) alloys the thermal profile defined in Table 4-1 remains the same except for dwells. Dwells at hot and cold temperature extremes can be carried out at the following two conditions depending on the reliability approach and user need:

a) ***Condition D10 (10 minute dwell)*** – This condition requires 10 minute dwells at the hot/cold temperature extremes. This is perhaps the most efficient accelerated thermal cycle profile as it induces the most strain energy per unit of time (considering the entire cycle) or per unit dwell time. Cycles-to-failure data generated under this condition should generally be used to make "stand-alone" life assessments for Pb-free solder joints, and not to make comparisons between the life of Pb-free and Sn-Pb joints. Only when damage accumulation is understood through accepted models can test results be used to determine the relative performance of Pb-free and Sn-Pb joints under product service conditions.

b) ***Condition D30+ (30 minutes or higher dwell)*** – This condition requires dwells of 30 minutes and higher (60 minutes) at the hot/cold temperature extremes in order to experimentally induce creep damage that may be somewhat comparable to lead-based solder. Modeling in conjunction with experimental data at different dwell times may be required to better define such a comparison.

For bismuth-tin (Bi-Sn) based solder alloys (e.g., 57Bi-42Sn-1Ag), the 0 - 100°C temperature cycle should be required, unless components plated with Sn-Pb solder are used. In this case, a -25 to +75°C temperature cycle is recommended. Cycle profiles other than these should not be considered acceptable for this class of Pb-free solders.

B.3.4 Recommendations to 4.2.2.1, PWB/PCB Surface Finish, Item 9 OSP or immersion silver (IAg) surface finish which is a Pb-free material should be used for testing of Pb-free solder joints. Sn-Pb HASL finish on the PWB should not be allowed for testing of Pb-free components and Pb-free solders. Other surface finishes may be used for manufacturer's internal data comparison only.

B.3.5 Recommendations to 5.4, Test Exemption Requirements Note that two additional requirements have been added to Table 4-3:

(1) Thermal cycle testing of solder joints should be required when the component terminal plating or solder ball alloy is changed:

Description	EXEMPT	Exemption Category A
Solder ball alloy, termination plating	[NEW] = [PQ 9701]	[NEW] = [PQ 9701]

(2) Thermal cycle testing of solder joints should be required when the solder paste alloy used for 2nd-level assembly is changed:

Description	EXEMPT	Exemption Category A
Solder paste materials	[NEW] = [PQ 9701]	[NEW] = [PQ 9701]

B.4 INFORMATION UPDATE SPECIFIC TO Pb-FREE SOLDER ALLOYS

B.4.1 Other Specification Revisions for Pb-Free This specification refers to many other standards associated with the manufacture of the test vehicle, from components and laminates to 2nd-level assembly and rework processes. Some of these standards are currently being modified by industry to account for the changes in manufacturing conditions required by the new Pb-free alloys. Modifications may be required to account for the higher 2nd-level manufacturing process temperatures required for Sn-Ag-Cu or other alloys, and the impact that this has on all the materials involved. The applicable modified document for Pb-free alloys should be used when they are available and the build process should be fully documented. Examples include the IPC-S-816, *SMT Process Guideline and Checklist*, the IPC-7711/21, *Rework and Repair Guide*, etc.

B.4.2 Solder Failure Mechanism Failure mechanisms defined in 3.6.2 may not be comparable with Pb-free alloys. Solder failure mechanisms may change at extremely hot and cold temperatures and if so, need to be validated.

In addition, the background information provided in 3.9 is valid for eutectic Sn-Pb solder alloy, as specifically mentioned in the first paragraph.

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